

In The Claims

Please amend the claims as follows:

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1. (Amended) An automated test equipment (ATE) comprising:

a tester-per-pin architecture having a plurality of individual decentralized per-pin testing units, wherein each per-pin testing unit is adapted for testing a respective pin of a device under test (DUT) by at least one of emitting stimulus response signals to said respective DUT-pin and receiving stimulus response signals from said respective DUT-pin, wherein during a testing sequence, the DUT is defined as one or more DUT-cores representing one or more functional units of said DUT and including one or more DUT-pins of said DUT; and

means for assigning, during said testing sequence, one or more of said per-pin testing units to one or more ATE-ports, whereby each ATE-port comprises one or more of said per-pin testing units and represents an independent functional testing unit for testing one or more of said DUT-cores during said testing sequence.

2. (Amended) The automated test equipment of claim 1, wherein said means for assigning comprises:

switching means for switching connections between one or more of said per-pin testing units and one or more of said DUT-pins, and

controlling means for controlling the switching of said switching means in accordance with the assigning of said one or more of the per-pin testing units to said one or more ATE-ports during said testing sequence.

3. (Amended) The automated test equipment of claim 1, wherein at least one of said ATE-ports comprises programming means for independently defining at least one of programming timing and a stimulus/response pattern.

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4. (Amended) The automated test equipment of claim 3, wherein said programming means comprises at least one of:

means for specifying cycle times of stimulus and response vectors for said at least one

ATE-port;

Sub B5 means for specifying a per-pin timing in terms of sets of available waveforms for each ATE-pin of the one ATE-port, whereby each waveform represents a sequence of events of various types occurring at specified instances in time;

means for specifying a pattern program for the one ATE-port;

means for specifying a per-pin vector data for each pin of the one ATE-port; and

means for specifying analogue set-up conditions for analogue pins of the one ATE-port.

5. (Amended) The automated test equipment of claim 3, wherein said programming means comprises:

main pattern programs for implementing access protocols to one or more of said DUT-cores through a shared set of per-pin testing units comprising one individual ATE-port comprising at least per-pin testing units that are part of the ATE-ports utilized to access said one or more DUT-cores, and

independent pattern programs for implementing stimulus and response patterns for each DUT-core of said one or more DUT-cores.

6. (Amended) The automated test equipment of claim 5, wherein said main pattern program comprises at least one of:

means for configuring said one individual ATE-port for activating said per-pin testing units thereof for accessing said one or more DUT-cores; and

means for selecting pattern data generated by pattern programs of said accessed DUT-cores during one testing sequence for testing said accessed DUT-cores.

7. (Amended) The automated test equipment of claim 3, wherein said programming means comprises:

specifying means for specifying an alias mapping between per-pin testing units for a plurality of said ATE-ports, for specifying at least one of timing information and a

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pattern program of one individual ATE-port to apply for the plurality of the ATE-ports for which the alias mapping is defined.

8. (Amended) The automated test equipment according to claim 1, further comprising specifying means for specifying overall test conditions for a test that concurrently operates on multiple ATE-ports.

9. (Amended) The automated test equipment of claim 8, wherein the specifying means comprises at least one of:

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means for determining a set of concurrently active ATE-ports during a defined testing sequence;

means for selecting the ATE-port test conditions for one or more ATE-pins, for selecting an ATE-port timing setup for one or more ATE-pins;

means for specifying global test conditions to express dependencies between pins of the DUT and the ATE; and

means for determining a multi-port pattern burst as a sequence of per-ATE-port: pattern programs for each ATE-port.

10. (Amended) A method for testing a device under test (DUT) with automated test equipment (ATE) comprising a tester-per-pin architecture having a plurality of individual decentralized per-pin testing units, wherein each per-pin testing unit is adapted for testing a respective pin of said DUT by at least one of emitting stimulus response signals to said respective DUT-pin and receiving stimulus response signals from said respective DUT-pin, said method comprising:

defining for a testing sequence said DUT as one or more DUT-cores: representing one or more functional units of said DUT and including one or more pins of said DUT; and

assigning during said testing sequence, one or more of said per-pin testing units to one or more ATE-ports, whereby each ATE-port comprises one or more of said per-pin testing units and represents an independent functional testing unit for testing one or more of said.

DUT-cores during said testing sequence.

11. (Amended) The method of claim 10, further comprising:

defining at least one of programming timing and a stimulus/response pattern for one or more of said ATE-ports.

12. (Amended) The method of claim 11, wherein defining at least one of programming timing and a stimulus/response pattern comprises at least one of:

specifying cycle times of stimulus and response vectors for the one ATE-port;

specifying a per-pin timing in terms of sets of available waveforms for each per-pin testing unit of the one ATE-port, whereby each waveform represents a sequence of events of various types occurring at specified instances in time;

specifying a pattern program for the one ATE-port, preferably specifying common sequencing instructions for all per-pin testing units of the one ATE-port;

specifying per-pin vector data for each per-pin testing unit of the one ATE-port; and

specifying analogue set-up conditions for analogue pins of the one ATE-port.

13. (Amended) The method according to claim 11, further comprising:

specifying overall test conditions for a test that concurrently operates on multiple ATE-ports.

14. (Amended) The method of claim 13, wherein specifying overall test conditions comprises:

determining a set of concurrently active ATE-ports during a defined testing sequence;

determining a multi-port pattern burst as a sequence of per-ATE-port pattern programs for each ATE-port.

means for assigning during said testing sequence, one or more of said per-pin testing units to one or more ATE-ports, whereby each ATE-port comprises one or more of said per-pin testing units and represents an independent functional testing unit for testing one or more of said DUT-cores during said testing sequence.